

MULTISTAGE DYNAMIC DOMINO CIRCUIT  
WITH INTERNALLY GENERATED DELAY RESET CLOCK

ABSTRACT

5           A multistage dynamic domino circuit includes a footed dynamic domino stage, a  
footless dynamic domino stage, and a internal delay circuit. The footed dynamic domino  
stage includes a first precharge circuit, evaluation logic, and a data output coupled to the  
evaluation logic. The footless dynamic domino stage includes evaluation logic including a  
data input coupled to the data output of the footed dynamic domino stage and a second  
10   precharge circuit. The second precharge circuit includes a first precharge device including a  
first current terminal and a control terminal coupled to a clock line. The second precharge  
circuit further includes a second precharge device including a first current terminal coupled to  
the first current terminal of first precharge device and a control terminal. The delay circuit  
includes an input coupled to the clock line and an output coupled to the control terminal of  
15   the second precharge device to provide a delayed version of a clock signal provided at the  
input of the delay circuit.